

CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Previously Presented) A system for overflow and saturation processing, comprising:

an adder, operatively connected to receive first and second operands, and connected to add the operands to produce a result of the added operands;

an accumulator, operatively connected to store at least a portion of the result of the added operands or at least a portion of a selected one of predetermined constants based on control signals;

guard bits, operatively connected to store the remaining portion of the result of the added operands or the remaining portion of the selected one of predetermined constants based on the control signals;

overflow logic operatively connected to the accumulator and to the guard bits so as to indicate overflow of the accumulator;

saturation logic, operatively connected to the adder, to the guard bits, and connected to provide the control signals based on at least a portion of the result of the added operands and at least a portion of the guard bits; and

logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison.

2. (Cancelled)

3. (Previously Presented) The system according to claim 1, wherein the saturation logic includes:

a selector operatively connected to selectively provide a one of the result of the added operands or a one of the predetermined constants based on the comparison.

4. (Previously Presented) The system according to claim 1, wherein the logic means includes:

means for providing the control signals in accordance with an enable signal and in accordance with the comparison.

5. (Previously Presented) The system according to claim 4, wherein the logic means further includes:

means, responsive to the comparison, for selectively providing the control signals so that the accumulator stores at least a portion of the result of the added operands and the guard bits store the remaining portion of the result of the added operands, or the accumulator stores at least a portion of a predetermined constant and the guard bits store the remaining portion of the predetermined constant.

6 - 7. (Cancelled)